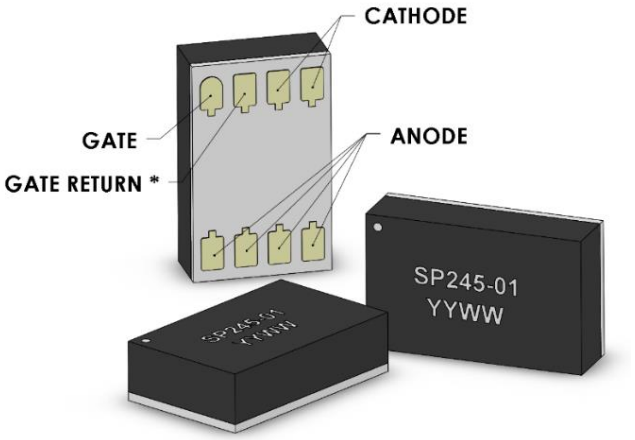
***NOTICE:* This product is export controlled**

The **SP245-01** is an advanced high-voltage current-controlled thyristor packaged in a **C-Pak** SMT package.

Like all Solidtron products, the internal semiconductor employs high cell density and an advanced planer termination design to achieve high peak current capability, low conduction loss, low off-state leakage, negligible turn-on delay jitter, and most importantly, extremely high turn-on dI/dt capability. It is ideally suited for a wide variety of capacitor discharge applications requiring precise timing and rapid energy transfer capability.

The **C-Pak** is a custom surface mount package in which the semiconductor is attached to a metalized ceramic substrate using 90Pb10Sn solder, wire bonded using 0.010" aluminum wire bonds, and then encapsulated using Hysol FP4653 epoxy. The **C-Pak** is specifically designed to be compliant with IPC 2221A Section 6.3 Electrical Clearance (any elevation).

The **SP245-01** replaces the CCSCP32N15. Like its predecessor, it is intended to replace triggered spark gaps of similar voltage and current ratings.



The **Gate Return pad provides a dedicated connection directly to the cathode of the semiconductor die. This connection consists of a single 0.010" aluminum bond wire.*

*Using the Gate Return pad as an independent gate driver return path reduces V=L*dI/dt induced stress on the gate driver components.*

With C-Pak Solidtron devices, the Gate Return pad may, alternatively, be used as an additional Cathode pad; however, its internal connection possesses only 40% of the I²t capability of each of the other Cathode pads. Using it in this fashion must be qualified by the customer for their specific application.

Key Product Features

- 1500V Repetitive Off-State Voltage
- V_{GK} = 0V = OFF
- 100 kA/µs dI/dt capability
- Low Turn-on and Conduction Losses
- < 100nSec Turn-on Delay Time
- 3.5kA Repetitive Surge Current

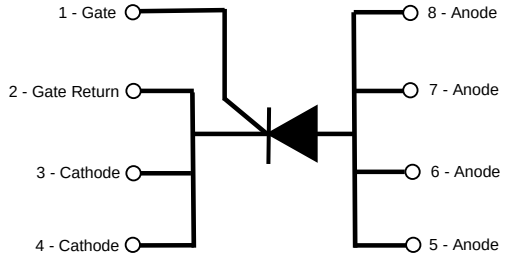


Table 1. Maximum Ratings	Symbol	Value	Units
Repetitive Peak Off-State Voltage	V_{DRM}	1500	V
Repetitive Peak Reverse Voltage	V_{RRM}	-10	V
Off-State Rate of Change of Voltage Immunity (V_D=1500V)	dv/dt	1000	V/µSec
Peak Non-Repetitive Surge Current (1/2 Sinusoid Pulse Duration =/<300nSec)	I_{TSM}	4000	A
Peak Repetitive Surge Current (1/2 Sinusoid Pulse Duration =/<300nSec)	I_{TRM}	3500	A
Rate of Change of Current	dI/dt	100	kA/µSec
Critical Capacitor Discharge Event Integral (Underdamped LCR Circuit) (Note 1.)	$I^2t_{CRITICAL}$	TBD	A^2sec
Repetitive Capacitor Discharge Event Integral (Underdamped LCR Circuit) (Note 1.)	$I^2t_{REPETITIVE}$	2	A^2sec
Continuous Gate-Cathode Reverse Voltage	V_{GKS}	-9	V
Forward Peak Gate Current (10µSec Duration)	I_{GM}	10	A
Required Off-State Gate-Cathode Voltage	V_{GDM}	0	V
Operating Junction Temperature Range	T_J	-55 to +125	°C
Maximum Soldering Installation Temperature *(See Moisture Sensitivity Caution)*		220	°C
Storage Temperature Range *(See Moisture Sensitivity & Solderability Cautions)*		-55 to +150	°C

Note 1. See Application Notes

Table 2. Electrical Characteristics

Parameter	Symbol	Test Conditions		Measurements Min	Typ	Max	Units
Anode to Cathode Breakdown Voltage	V_{BR}	V_{GK}= 0V, I_D=100µA, $T_C \leq 125°C$		1500			V
Anode-Cathode Forward Off-State Current *See Figure 2.*	I_{DRM}	V_{GK}= 0V, V_D=1500V	T_C=-55°C			60	nA
			T_C=25°C		10	100	nA
			T_C=85°C		190	1000	nA
			T_C=125°C		5	10	µA
Reverse Bias Gate-Cathode Breakdown Voltage	V_{GRRM}	I_{GM}=150µA, $T_C \leq 125°C$		9	10		V
Nine Volt Reverse Bias Gate-Cathode Leakage Current *See Figure 1.*	I_{GM}	V_{GK}= -9V	T_C=25°C		28		µA
			T_C=85°C		57		µA
			T_C=125°C		80		µA
Two Volt Reverse Bias Gate-Cathode Leakage Current *See Figure 1.*	I_{GM}	V_{GK}= -2V	T_C=25°C		0.8	2	µA
			T_C=85°C		1.9	4	µA
			T_C=125°C		2.4	6	µA
Gate Trigger Voltage	V_{GT}	V_D= 12V, I_D=1mA	T_C=25°C	450	500		mV
			T_C=85°C	250	350		mV
			T_C=125°C	200	250		mV
Gate Trigger Current	I_{GT}	V_D= 12V, I_D=1mA, $T_C \leq 125°C$				100	µA
Turn-on Delay Time	$t_{d(ON)}$	0.15µF Capacitor Discharge, T_C=25°C, I_{GT}= 500mA, V_{DD}=1200V, L_S=15nH, R_S=0.010Ω=CVR			30	60	nSec
Rate of Change of Current	dI/dt				65		kA/µsec
Capacitor Discharge Event Integral	I^2t				1.38		A^2sec
Peak Anode Current	I_{DM}				3.2		kA

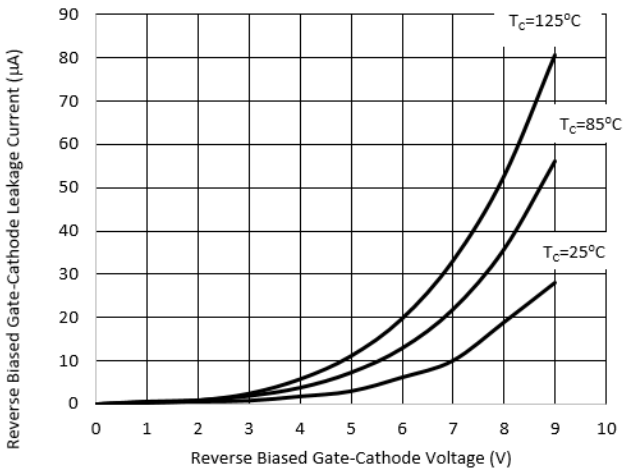


Figure 1. Typical Reverse Biased Gate-Cathode Leakage Characteristic

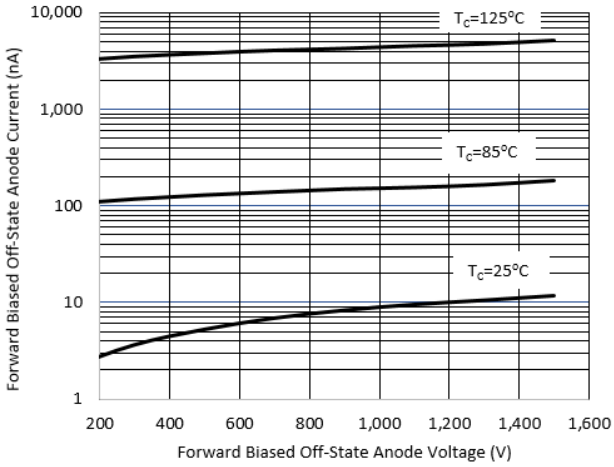
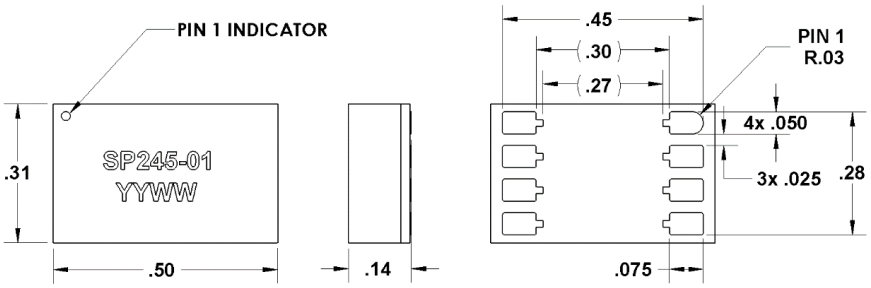


Figure 2. Typical Forward Biased Off-State Anode-Cathode Leakage Characteristic

Markings and Dimensions



DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED:
TWO PLACE DECIMAL +/- 0.010"
THREE PLACE DECIMAL +/- 0.004"

PART NUMBER
SP = SILICON POWER
245 = CHIP TYPE
-01 = PACKAGE TYPE

DATE CODE
YY = LAST 2 DIGITS OF CALENDAR YEAR
WW = WORK WEEK

ESD Sensitivity

THIS PRODUCT SHOULD BE HANDLED AS AN ESD SENSITIVE DEVICE. OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS (REF. JESD625).

IMPROPER HANDLING OF THIS DEVICE MAY PERMANENTLY DAMAGE THE DEVICE AND RENDER IT UNUSABLE.

Moisture Sensitivity

SP245-01 MSL testing IAW IPC/JEDEC J-STD-020D.1 will be completed when two non-consecutive date codes of this product are available for testing. This datasheet will be revised to include the results at that time. Based on previous CCSCP32N15 C-Pak MSL test results, it is recommended these parts be handled as MSL level 5A until a revision is issued.

In accordance with **IPC/JEDEC J-STD-033**, **C-Pak** products are dry-baked then packed in a Moisture Barrier Bag (MBB) containing desiccant and a Humidity Indicator Card (HIC). When the Moisture Barrier Bag is opened or compromised refer to **IPC/JEDEC J-STD-033** for proper HIC interpretation, floor life and storage procedures.

Although **IPC/JEDEC J-STD-033** prescribes specific dry-baking temperatures and times, caution is advised as additional baking of **C-Pak** SMD packages may cause oxidation and/or intermetallic growth of the terminations which may result in solderability problems during board installation. The temperature and time for baking this SMD package should, therefore, be limited with solderability considerations in mind. If available, it is recommended C-Paks be baked in a nitrogen or vacuum oven to limit exposure to oxygen during the baking process.

Solderability

The component pads of the **C-Pak**, *although gold plated*, **are subject to oxidation** of the underlying nickel if handled or stored inappropriately**.** Prolonged exposure to circumstances known to promote nickel oxidation should be avoided; otherwise, solderability of the **C-Pak** will be compromised.

Product Qualifications/Certifications/Classifications

Planned or Underway

- Solderability per IPC J-STD-002
- MSL-5A per IPC/JEDEC J-STD-020D.1
- ESD-HBM (Human Body Model) classification per Mil-STD-883
- ESD-CDM (Charged Device Model) classification per ANSI/ESDA/JEDEC/JS-002-2014

Application Notes

Topics Under Development

- Capacitor Discharge Event Integral (I^2t)
- Triggering a CCS Device - Theory of Operation
- Gate Driver design for the CCS Device
  - Circuits & Critical Layout Considerations

Table 3. Typical Application Parameters

	Value	Units
Off-State Anode Voltage (<1 hour)	1250	V
Repetitive Peak Forward Anode Current (**1/2 Cycle Pulse Width = 160nSec**)	2.7	kA
Repetitive Peak Reverse Anode Current (**1/2 Cycle Pulse Width = 160nSec**)	2.2	kA
Off-State Rate of Change of Voltage (dv/dt) immunity	≤200	V/mSec
Operational Case Temperature	-55 to 85	°C
Rate of Change of Anode Current (dI/dt)	65	kA/µSec
Peak Forward Gate Current (≤20uSec pulse)	500	mA
Event Repetition Rate	<1	Hz